WHAT IS CLAIMED IS:

1. A content addressable memory (CAM) device configured with binary CAM cells capable of holding binary data, the CAM device capable of being used either as a binary CAM device with the binary CAM cells being used as binary CAM cells or as a ternary CAM device with the binary CAM cells being used as ternary CAM cells capable of holding ternary data in a way in which, in each pair of two bits of the binary CAM cells, three states, "0," "1," and "X (don't care)" are assigned to four states, "00," "01," "10," and "11," expressed by two-bit data stored in the pair.

2. A CAM device according to Claim 1, wherein each of the pairs of the binary CAM cells constituting the ternary CAM cells is included in two different CAM words.

3. A CAM device according to Claim 2, wherein each of the pairs of the binary CAM cells constituting the ternary CAM cells has the same bit number.

4. A CAM device according to Claim 2, wherein the two different CAM words are an even word having an even word number and an odd word having the odd word number following the even word number.

5. A CAM device according to Claim 4, wherein each of the pairs of the binary CAM cells constituting the ternary CAM cells is included in an even word and the odd word following the even word and has the same bit number.

6. A CAM device according to Claim 1, wherein each of the pairs of the binary CAM cells constituting the ternary CAM cells is included in one CAM word.

7. A CAM device according to Claim 6, wherein each of the pairs of the binary CAM cells constituting the ternary CAM cells has an even bit number and an odd bit number adjacent to each other in one CAM word.

8. A CAM device according to Claim 1, wherein, during a search operation, a pair of search bit lines used for one binary CAM cell of each of the pairs of the binary CAM cells and a pair of search bit lines used for the other binary CAM cell are separately controlled.

9. A CAM device according to Claim 1, wherein, when the CAM device is used as a ternary CAM device, data conversion processing is applied to storage data, mask data, and search data between external data (logical data) and

internal data (physical data).

10. A structure method for a content addressable memory (CAM) device configured with binary CAM cells capable of holding binary data, wherein, in each pair of two bits of the binary CAM cells, three states, "0," "1," and "X (don't care)" are assigned to four states, "00," "01," "10," and "11," expressed by two-bit data stored in the pair to implement the function of a ternary CAM cell capable of holding ternary data.

11. A content addressable memory (CAM) device comprising:

a CAM array including a plurality of CAM words each formed of binary CAM cells; and

binary/ternary setting means for making a setting of a case in which the binary CAM cells are used as binary CAM cells or a setting of a case in which each pair of two bits of the binary CAM cells is used as a ternary cell.

12. A CAM device according to Claim 11, further comprising a logical-data/physical-data conversion circuit for converting logical data input from the outside to physical data used in the inside of the CAM device according to a setting made by the binary/ternary setting means.

13. A CAM device according to Claim 12, wherein the logical-data/physical-data conversion circuit comprises:

a write-in-data converter for converting storage data and mask data for ternary CAM cells, input from the outside to data to be stored in each pair of two bits of binary CAM cells;

a search-data converter for converting search data input from the outside to a search bit line signal for each pair of two bits of binary CAM cells; and

a read-out-data converter for converting physical data read from each pair of two bits of binary CAM cells, constituting a ternary CAM cell, to logical data.

14. A CAM device according to Claim 11, wherein the binary/ternary setting means is a terminal for inputting a binary/ternary setting signal from the outside.

15. A CAM device according to Claim 12, wherein the binary/ternary setting means is a terminal for inputting a binary/ternary setting signal from the outside.

16. A CAM device according to Claim 13, wherein the binary/ternary setting means is a terminal for inputting a binary/ternary setting signal from the outside.

17. A CAM device according to Claim 11, wherein the binary/ternary setting means is an internal register for holding a binary/ternary setting signal.

18. A CAM device according to Claim 12, wherein the binary/ternary setting means is an internal register for holding a binary/ternary setting signal.

19. A CAM device according to Claim 13, wherein the binary/ternary setting means is an internal register for holding a binary/ternary setting signal.

20. A CAM device according to Claim 16, further comprising an array I/O circuit for sending write-in data and search data output from the logical-data/physical-data conversion circuit to CAM cells and for sending data read from the CAM cells to the logical-data/physical-data conversion circuit, according to the binary/ternary setting means.

21. A CAM device according to Claim 19, further comprising an array I/O circuit for sending write-in data and search data output from the logical-data/physical-data conversion circuit to CAM cells and for sending data read

from the CAM cells to the logical-data/physical-data conversion circuit, according to the binary/ternary setting means.

22. A CAM device according to Claim 20,

wherein the CAM array is formed of an even CAM array including CAM words having even word numbers and an odd CAM array including CAM words having odd word numbers;

a match line of one word included in the even CAM array is coupled with a match line of the word having the word number following the one word, included in the odd CAM array, by a logic circuit; and

a match output of a binary CAM word or a match output of a ternary CAM word is output according to a signal of the binary/ternary setting means.

23. A CAM device according to Claim 22, wherein the array I/O circuit is provided for each of the even CAM array and the odd CAM array.

24. A CAM device according to Claim 23, further comprising:

an external data input line made by integrating a data line for search data input from the outside, a data line for storage data input from the outside, and a data line for

mask data input from the outside, for inputting each of the data in a time division manner; and

an input register for holding data input first of the storage data and the mask data, and for outputting held data to the logical-data/physical-data conversion circuit together with the data input last.

25. A CAM device according to Claim 24, further comprising a selector connected at its inputs to a data line for read storage data and to a data line for read mask data, both data output from the logical-data/physical-data conversion circuit, for outputting each of the data in a time division manner.

26. A CAM device according to Claim 25, further comprising:

a selector for receiving write-in data for an even word and search data for the even word, both data output from the logical-data/physical-data conversion circuit, and for outputting one of the data to the even array I/O circuit according to a data writing operation or a data search operation; and

a selector for receiving write-in data for an odd word and search data for the odd word, both data output from the logical-data/physical-data conversion circuit, and for

outputting one of the data to the odd array I/O circuit according to a data writing operation or a data search operation.